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09/802,356	03/08/2001	Hidekazu Watanabe	80398P346	7422

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EXAMINER	
CERULLO, JEREMY S	

ART UNIT	PAPER NUMBER
2112	

DATE MAILED: 12/09/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/802,356	WATANABE ET AL.	
	Examiner	Art Unit	
	Jeremy S. Cerullo	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 March 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 March 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because reference character "230" has been used to designate both the data path from Bus Controller K to Slave Device K1 and the data path from Bus Controller 2 to Slave Device 21. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

2. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: 220 and 240. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing

figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

3. The disclosure is objected to because of the following informalities:

In Paragraphs [0013], [0016], and [0017], "140_{jk} (j = 1,..., K, k = 1,...,L, 1,...M, 1,...,K)" should apparently be "140_{jk} (j = 1, ..., K, k = 1, ..., L, 1, ..., M, 1,...,P)" (Note the comma added before M and that the second K has been changed to P);

In the 4th line of Paragraph [0021], "135_N" should apparently be "130_K" and "135K" should apparently be "135_K"; and

In Paragraph [0036], all references to "multiplexer 420" should apparently be changed to "multiplexer 410".

Appropriate correction is required.

Claim Objections

4. Claim 30 objected to because of the following informalities: As written, Claim 30 is dependent upon Claim 5. As Claim 5 is drawn to an apparatus and not a system, and given the manner in which the other claims are arranged, the examiner assumes that Claim 30 is meant to be dependent upon Claim 25, and has interpreted the Claim 30 in such a way for reasons of applying prior art. Appropriate correction is required.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

7. Claims 1-2 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 4,698,753 (Hubbins). Hubbins teaches an arbiter coupled to first and second processors to generate an arbitration select signal (Figure 1). Hubbins also teaches a multiplexer coupled to the first and second processors and to a slave (in this case memory). While Hubbins does not explicitly teach that there is a plurality of slave buses, he does teach that several devices can be used in parallel (Abstract). It would be obvious to one of ordinary skill in the art at the time of the invention to connect multiple arbiter/multiplexer units to the first and second processors. One would be motivated to do so in order to allow for independent access to the slaves by each processor.

8. As for Claim 2, Hubbins also teaches that the device access information provided to the slave may be write data. (Column 3, Line 59 – Column 4, Line 22)

9. Claims 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hubbins as applied to claims 1-2 above, and further in view of U.S. Patent No. 5,590,369 (Burgess). Burgess teaches the additional limitation of an address decoder (Figure 1, Item 84) that decodes the slave address (Figure 1, Item 80) and generates a device select signal (Figure 1, Item 88). See Column 6, Lines 9-35 of Burgess. It would have been obvious to one of ordinary skill in the art at the time of the invention to use an address decoder as taught by Burgess in the apparatus of Hubbins. The motivation for doing so would be to allow for multiple slaves on the slave bus, in addition to the RAM of Hubbins.

10. Claims 4-5 and 7-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hubbins and Burgess as applied to claim 3 above, and further in view of U.S. Patent No. 5,453,737 (Opoczynski). Opoczynski teaches a selector (multiplexer) that selects data from multiple data buses for I/O (Figure 3, Item 46). Multiplexer 21 of Figure 2 of Hubbins is bi-directional to allow for reads and writes to memory, so it performs the functions of a multiplexer and a de-multiplexer. Therefore, Hubbins teaches the use of de-multiplexer to provide the bus response information to one of the first and second processors. It would have been obvious to one of ordinary skill in the art at the time of the invention to include the selector of Opoczynski in the apparatus of Hubbins and Burgess. One would have been motivated to do so in order to further support multiple slaves on the slave bus, in addition to the RAM of Hubbins.

11. As for Claim 5, Hubbins also teaches that the device access information provided to the slave may be write data. (Column 3, Line 59 – Column 4, Line 22)

12. As for Claim 7, Hubbins teaches that a DMA can be used as a host (Column 11, Lines 29-37).

13. As for Claim 8, Hubbins teaches that a microprocessor can be one of the devices connected as a processor (Figure 12 and Column 11, Lines 13-28).

14. As for Claim 9, Hubbins teaches that the first slave device is a memory device (Figure 1).

15. As for Claim 10, Hubbins teaches a homogeneous set (all memory devices) (Figure 1).

16. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hubbins, Bugress, and Opoczynski as applied to claims 4-5 and 7-10 above, and further in view of U.S. Patent No. 5,717,895 (Leedom). Leedom teaches access to common memory by various devices through a common memory interface (Figure 1). It would have been obvious to one of ordinary skill in the art at the time of the invention to use the common memory and common memory interface of Leedom in the system taught by Hubbins, Bugress, and Opoczynski. One would have been motivated to do so in order to allow the various slave devices access to data that would need to be shared.

17. Claims 11-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 4,698,753 (Hubbins). Hubbins teaches an arbiter coupled to first and second processors to generate an arbitration select signal (Figure 1). Hubbins also

teaches a multiplexer for providing device access information coupled to the first and second processors and to a slave (in this case memory). While Hubbins does not explicitly teach that there is a plurality of slave buses, he does teach that several devices can be used in parallel (Abstract). It would be obvious to one of ordinary skill in the art at the time of the invention to connect multiple arbiter/multiplexer units to the first and second processors. One would be motivated to do so in order to allow for independent access to the slaves by each processor.

18. As for Claim 22, Hubbins also teaches that the device access information provided to the slave may be write data. (Column 3, Line 59 – Column 4, Line 22)

19. Claims 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hubbins as applied to claims 11-12 above, and further in view of U.S. Patent No. 5,590,369 (Burgess). Burgess teaches the additional limitation of an address decoder (Figure 1, Item 84) that decodes the slave address (Figure 1, Item 80) and generates a device select signal (Figure 1, Item 88). See Column 6, Lines 9-35 of Burgess. It would have been obvious to one of ordinary skill in the art at the time of the invention to use an address decoder as taught by Burgess in the apparatus of Hubbins. The motivation for doing so would be to allow for multiple slaves on the slave bus, in addition to the RAM of Hubbins.

20. Claims 14-15 and 17-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hubbins and Burgess as applied to claim 13 above, and further in view of U.S. Patent No. 5,453,737 (Opoczynski). Opoczynski teaches a selector (multiplexer) that selects data from multiple data buses for I/O (Figure 3, Item 46).

Multiplexer 21 of Figure 2 of Hubbins is bi-directional to allow for reads and writes to memory, so it performs the functions of a multiplexer and a de-multiplexer. Therefore, Hubbins teaches the use of de-multiplexer to provide the bus response information to one of the first and second processors. It would have been obvious to one of ordinary skill in the art at the time of the invention to include the use of the selector of Opoczynski in the apparatus of Hubbins and Burgess. One would have been motivated to do so in order to further support multiple slaves on the slave bus, in addition to the RAM of Hubbins.

21. As for Claim 15, Hubbins also teaches that the device access information provided to the slave may be write data. (Column 3, Line 59 – Column 4, Line 22)

22. As for Claim 17, Hubbins teaches that a DMA can be used as a host (Column 11, Lines 29-37).

23. As for Claim 18, Hubbins teaches that a microprocessor can be one of the devices connected as a processor (Figure 12 and Column 11, Lines 13-28).

24. As for Claim 19, Hubbins teaches that the first slave device is a memory device (Figure 1).

25. As for Claim 20, Hubbins teaches a homogeneous set (all memory devices) (Figure 1).

26. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hubbins, Bugress, and Opoczynski as applied to claims 14-15 and 17-20 above, and further in view of U.S. Patent No. 5,717,895 (Leedom). Leedom teaches access to common memory by various devices through a common memory interface (Figure 1). It would

have been obvious to one of ordinary skill in the art at the time of the invention to use the common memory and common memory interface of Leedom in the system taught by Hubbins, Bugress, and Opoczynski. One would have been motivated to do so in order to allow the various slave devices access to data that would need to be shared.

27. Claims 21-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 4,698,753 (Hubbins). Hubbins teaches an arbiter coupled to first and second processors to generate an arbitration select signal (Figure 1). Hubbins also teaches a multiplexer for providing device access information coupled to the first and second processors and to a slave (in this case memory). While Hubbins does not explicitly teach that there is a plurality of slave buses, he does teach that several devices can be used in parallel (Abstract). It would be obvious to one of ordinary skill in the art at the time of the invention to combine multiple arbiter/multiplexer units (bus controllers) to the first and second processors in an interface circuit. One would be motivated to do so in order to allow for independent access to the slaves by each processor.

28. As for Claim 22, Hubbins also teaches that the device access information provided to the slave may be write data. (Column 3, Line 59 – Column 4, Line 22)

29. Claims 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hubbins as applied to claims 21-22 above, and further in view of U.S. Patent No. 5,590,369 (Burgess). Burgess teaches the additional limitation of an address decoder (Figure 1, Item 84) that decodes the slave address (Figure 1, Item 80) and generates a

device select signal (Figure 1, Item 88). See Column 6, Lines 9-35 of Burgess. It would have been obvious to one of ordinary skill in the art at the time of the invention to use an address decoder as taught by Burgess in the apparatus of Hubbins. The motivation for doing so would be to allow for multiple slaves on the slave bus, in addition to the RAM of Hubbins.

30. Claims 24-25 and 27-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hubbins and Burgess as applied to claim 3 above, and further in view of U.S. Patent No. 5,453,737 (Opoczynski). Opoczynski teaches a selector (multiplexer) that selects data from multiple data buses for I/O (Figure 3, Item 46). Multiplexer 21 of Figure 2 of Hubbins is bi-directional to allow for reads and writes to memory, so it performs the functions of a multiplexer and a de-multiplexer. Therefore, Hubbins teaches the use of de-multiplexer to provide the bus response information to one of the first and second processors. It would have been obvious to one of ordinary skill in the art at the time of the invention to include the selector of Opoczynski in the apparatus of Hubbins and Burgess. One would have been motivated to do so in order to further support multiple slaves on the slave bus, in addition to the RAM of Hubbins.

31. As for Claim 25, Hubbins also teaches that the device access information provided to the slave may be write data. (Column 3, Line 59 – Column 4, Line 22)

32. As for Claim 27, Hubbins teaches that a DMA can be used as a host (Column 11, Lines 29-37).

33. As for Claim 28, Hubbins teaches that a microprocessor can be one of the devices connected as a processor (Figure 12 and Column 11, Lines 13-28).

34. As for Claim 29, Hubbins teaches that the first slave device is a memory device (Figure 1).

35. As for Claim 30, Hubbins teaches a homogeneous set (all memory devices) (Figure 1).

36. Claim 26 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hubbins, Bugress, and Opoczynski as applied to claims 24-25 and 27-30 above, and further in view of U.S. Patent No. 5,717,895 (Leedom). Leedom teaches access to common memory by various devices through a common memory interface (Figure 1). It would have been obvious to one of ordinary skill in the art at the time of the invention to use the common memory and common memory interface of Leedom in the system taught by Hubbins, Bugress, and Opoczynski. One would have been motivated to do so in order to allow the various slave devices access to data that would need to be shared.

Conclusion

37. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. U.S. Patent No. 5,598,542 (Leung), U.S. Patent No. 6,233,635 (Son), U.S. Patent No. 6,275,890 (Lee), and U.S. Patent Application Publication No. 2002/0010822 (Kim).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeremy S. Cerullo whose telephone number is (571)

272-3634. The examiner can normally be reached on Monday - Thursday, 7:00-4:30; Alternate Fridays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark H. Rinehart can be reached on (571) 272-3632. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JSC